UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,808,976 B1
APPLICATION NO. : 09/652714
DATED : October 26, 2004
INVENTOR(S) : Vishnu K. Agarwal

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column, Line	Reads	Should Read
Column 2, Line 9	"WN_x/SiO_2 polysilicon"	--WN_x/SiO_2/polysilicon
Column 2, Line 15	"Wn_x,"	--WN_x--
Column 3, Line 16	"In yet another"	--Yet another--
Column 6, Line 55	"tantalum pentoxide"	--the tantalum pentoxide--
Column 8, Line 1	"process describe above"	--processed described above--
Column 10, Line 59	Insert claims 27 & 28 as follows:	--27. The method in claim **22** further comprising depositing a plug on which the first conductive layer is thereafter deposited, and wherein exposing the second conductive layer to a thermal process comprises flowing the second conductive layer.

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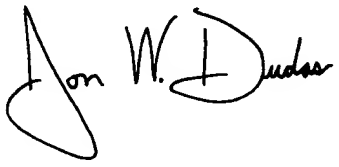
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

28. The method in claim **22**, wherein exposing the conductive layer to a thermal process comprises exposing the conductive layer to an alloy process.--

Signed and Sealed this

Eighth Day of January, 2008



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Director of the United States Patent and Trademark Office